JBE-1603010102010200 Seat No. _____

M. Sc. (Sem. I) (CBCS) Examination

December - 2019

Physics : CT - 02

(Solid State Electronic Devices & Circuits) (New Course)

Time : $2\frac{1}{2}$ Hours] [Total Marks : **70**

Instructions : (1) All questions are compulsory.
(2) Figure in the right indicate marks.

1 Answer the following : (any **seven**) **14**

(a) Write Schokley's equation which relates the gate to source bias voltage and drain current for JFET.

(b) Differentiate : Avalanche and Zener breakdown mechanisms.

(c) Which logic family has the lowest power dissipation ?

(d) Distinguish between direct and indirect band gap materials.

(e) Calculate transconductance (g_m) of JFET having the parameters : $I_{DSS} = 18$ mA, $V_P = -4$V for drain current $I_D = 2$ mA.

(f) Calculate wavelength $\left(\lambda_g\right)$ of light emission for GaAs having band gap energy $E_g = 1.44$ eV.

(g) Prove that sum of all the minterms of a Boolean function of N-variable is 1.

(h) What is the relation between photometric unit lumen and radiometric unit watt ?

(i) What is the operational principle of Solar cell ?

(j) Simplify the following Boolean function :
$F = (A+B)' \cdot (A'+B')'$

2 Answer the following : (any **two**) **14**

(a) Compare: BJT and JFET. Describe the construction of N-channel JFET and explain its drain-source characteristics.

(b) For JFET, using the Schokley's equation and transconductance $g_m = \frac{dI_D}{dV_{GS}}$, show that

$g_m = \frac{2\sqrt{I_{DSS}}\sqrt{I_D}}{|V_P|}$ (I_{DSS} is saturated drain current with $V_{GS} = 0$, V_P = Pinch off voltage, I_D = drain current, and V_{GS} = gate to source voltage)

(c) Write a detailed note on JFET source follower.

3 Answer the following : **14**

(a) Draw the circuit of 2-input NAND gate using transistor-transistor (TTL) logic and explain its operation . Explain current sinking and current sourcing in TTL.

(b) Write a detailed note on MOS logic family.

OR

3 Answer the following : **14**

(a) A logic circuit having three inputs should produce high output when its input binary number has majority of bits high. Design the logic circuit using K-Map and draw the circuit using AND-OR implementation.

(b) Simplify the following Boolean function using Karnaugh Map method : $F(w, x, y, z) = \sum(1, 3, 7, 11, 15)$ and don't cares are : $d(w, x, y, z) = \sum(5, 9, 13)$.

4 Answer the following : (any **two**) **14**

(a) Draw basic structure and symbol of Silicon Controlled Rectifier. Explain the current voltage characteristics of SCR and derive anode current expression for forward blocking state.

(b) Explain the physics of light emission in LED. Explain in detail radiative recombination processes. Give a brief note on LED materials.

(c) Discuss in detail the physics of photoconductive detectors hence derive expression for photoconductive gain. What are the photoconductive materials ?

5 Write short notes on any **two** : **14**

(a) TRIAC

(b) Thermistors

(c) Zener diode voltage regulator

(d) UJT relaxation oscillator.